

Hex Inverted Buffers with Open-Collector Outputs

This device contains hex inverted buffers with open-collector. It performs the Boolean function $Y=A$ in positive Logic.

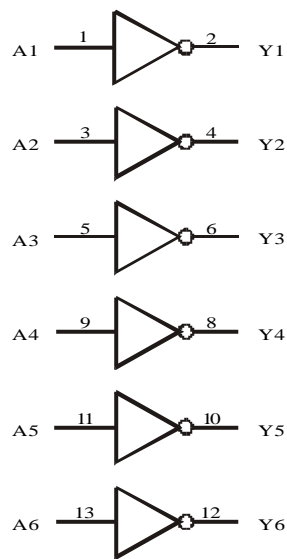
- High Output Voltage (30 V)
- High Speed ($t_{PD} = 8.5$ ns typical)
- Low Power Dissipation ($P_D = 18$ mW per Gate)

N SUFFIX PLASTIC

D SUFFIX SOIC

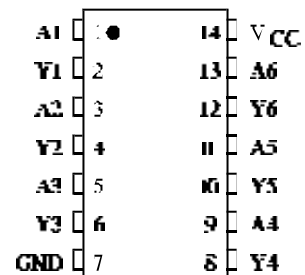
ORDERING INFORMATION
 SL74LS06N Plastic
 SL74LS06D SOIC
 $T_A = 0^\circ$ to 70° C for all packages

LOGIC DIAGRAM



PIN 14 = V_{CC}
 PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs	Output
A	Y
H	L
L	H

SL74LS06

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	7.0	V
V _{IN}	Input Voltage	5.5	V
V _{OUT}	Output Voltage	30	V
T _{stg}	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	4.75	5.25	V
V _{IH}	High Level Input Voltage	2.0		V
V _{IL}	Low Level Input Voltage		0.8	V
V _{OH}	High Level Output Voltage		30	V
I _{OL}	Low Level Output Current		40	mA
T _A	Ambient Temperature Range	0	+70	°C

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit	
			Min	Max		
V _{IK}	Input Clamp Voltage	V _{CC} = min, I _{IN} = -18 mA		-1.5	V	
I _{OH}	High Level Output Current	V _{CC} = min, V _{OH} = max		250	μA	
V _{OL}	Low Level Output Voltage	V _{CC} = min, I _{OL} = 16 mA		0.4	V	
		V _{CC} = min, I _{OL} = 40 mA		0.7		
I _{IH}	High Level Input Current	V _{CC} = max, V _{IN} = 2.7 V		20	μA	
		V _{CC} = max, V _{IN} = 5.5 V		1	mA	
I _{IL}	Low Level Input Current	V _{CC} = max, V _{IN} = 0.4 V		-0.2	mA	
I _{CC}	Supply Current	V _{CC} = max	Total with outputs high		18	mA
			Total with outputs low		60	

AC ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $C_L = 15\text{ pF}$, $R_L = 110\ \Omega$, $t_r = 15\text{ ns}$, $t_f = 6.0\text{ ns}$)

Symbol	Parameter	Min	Max	Unit
t_{PLH}	Propagation Delay, Input A to Output Y		15	ns
t_{PHL}	Propagation Delay, Input A to Output Y		20	ns

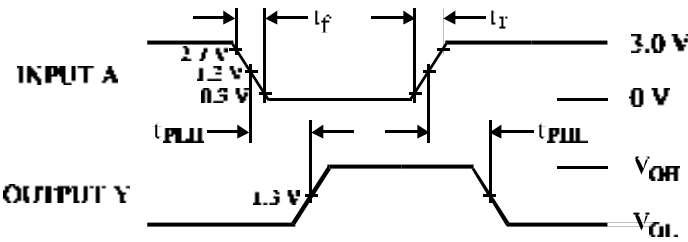
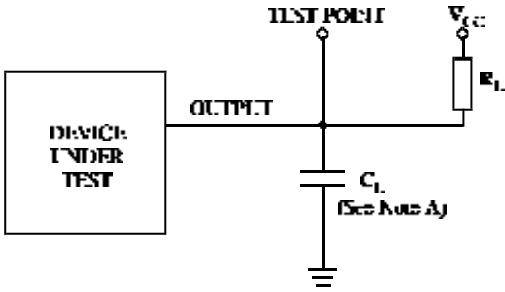


Figure 1. Switching Waveforms



NOTE A. C_L includes probe and jig capacitance.

Figure 2. Test Circuit